tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode.

Please add new claims 12 - 14 to read as follows:

-- 12. A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness of at most 3nm;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate

on both sides of said floating gate electrode; and

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a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode.

13. A semiconductor memory according to claim 12, wherein said tunneling insulating film has a thickness of at least 2 nm.

A 2 cont

B4

14. A semiconductor memory comprising:

a semiconductor substrate;

a tunneling insulating film formed on a partial surface area of said semiconductor substrate, said tunneling insulating film having a thinness enough to transmit carriers therethrough by a tunneling phenomenon;

a floating gate electrode formed on said tunneling insulating film;

a gate insulating film covering a side wall of said floating gate electrode and a partial surface area of said semiconductor substrate on both sides of said floating gate electrode, said gate insulating film having a thickness not allowing carriers to transmit therethrough by the tunneling phenomenon;

a first control gate electrode disposed on said gate insulating film over the side wall of said floating gate electrode and over a partial surface area of said semiconductor substrate on both sides of said floating gate electrode; and

B4 A cont

a pair of impurity doped regions formed in a surface layer of said semiconductor substrate on both sides of a gate structure including said floating gate electrode and said first control gate electrode,

wherein a surface layer of said semiconductor substrate under said first control gate electrode has a conductivity opposite to that of said impurity doped regions. --